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EXAMINER	
TORRES, JUAN A	

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2631	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,797	ADKISSON, RICHARD W.	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☒ Claim(s) *1-12 and 14-19* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed on 04/11/2005 have been fully considered but they are not persuasive.

As per claim 1:

The Applicant contends, "Applicant respectfully traverses the pending 103 rejection of the base claim 1 as applied above and offers the following arguments in support. As set forth in the base claim 1, an embodiment of the present invention is directed to a SYNC pulse compensation apparatus that comprises, inter alia, a sampling/compensation circuit operable to condition a SYNC pulse signal. The Price reference is directed to a digital information handling system that employs subsystems operating with different clock frequencies and which are capable of transferring data between one another. The applied language of the Price reference at column 9 lines 37-42 and lines 65-67 does not teach, suggest or even remotely allude to a sampling compensation circuit operable to condition a SYNC signal. Rather, it merely displaces that a first synchronization circuit 136 generates a synchronization signal called SYNC READY to synchronize data transfer from Memory Controller 126 in a second subsystem clock environment to system Processor 124 in a first subsystem via System Processor Bus 128. Applicant respectfully submits that generation of SYNC READY signal does not anticipate or suggest conditioning a SYNC pulse as currently claimed. As set forth in the specification of the present patent application, conditioning of the SYNC pulse is performed by the sampling compensation circuit in order to remove

certain anomalous conditions in the SYNC pulse, e.g., a lost SYNC pulse, a duplicate pulse condition, etc. See Specification at page 17, line 16 to page 18, line 11".

The Examiner disagrees and asserts, that, as indicated in the previous office action, that Price discloses, *inter alia*, "for each clock frame period, the clock generation circuit generates a first sync pulse to signal the first subsystem that timing alignment is established between the first clock and the second clock and a second sync pulse to signal the second subsystem that timing alignment between the first clock and the second clock has occurred" (Price column 2 lines 18-29). And also "Clock Generation Circuit 118 produces multiple clock signals having different frequencies and a fixed predetermined timing relationship. Clock Generation Circuit 118 also produces multiple synchronization pulses which correspond to the timing relationship of the clock signals it produces. The term "fixed predetermined timing relationship" as used herein indicates that periodically, the rising edge or falling edge of the first clock signal is separated in time by a fixed predetermined period of time from the respective rising edge or falling edge of the second clock signal" (column 9 lines 65-67). This is a compensation circuit operable to condition a SYNC signal bases on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion, as claimed.

The Applicant contends, "Moreover, as admitted in the pending Office Action, the Price reference does not disclose a jitter cycle delay compensation circuit as recited in the base claim 1. Application of the Kurd reference is of no avail, however, when applied as a secondary reference in combination with the Price reference in order to

provide a basis for obviousness. It is well known that to establish obviousness three basic criteria must be met. First, there must be some suggestion or motivation to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the combined references must teach or suggest all the claim limitations. See MPEP :2143. Applicant respectfully contends that there is no suggestion or motivation in either of the applied references to carbine the teachings

The Examiner disagrees and asserts, that, as indicated in the previous office action, the suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18).

The Applicant contends, "therein so as to achieve the claimed invention which involves, inter alia, (i) a sampling compensation circuit operable to condition a SYNC pulse signal; arid (ii) a jitter cycle delay compensation circuit coupled to the sampling compensation circuit, wherein the jitter cycle delay compensation circuit operates to tap the SYNC pulse signal after a predetermined delay based on a skew difference between first and second clock signals. The Kurd reference is directed to digital clock skew detection and phase alignment between two digital clock signals that are copies of each other. See column 1, lines 11-24. As such, there is no teaching or suggestion in the Kurd reference with regard to a SYNC sampling compensation circuit operable to condition a SYNC pulse signal as discussed above. Figure 6 of the Kurd reference show a circuit schematic of an application of a skew detection circuit for minimizing skew between different clock domains. Two separate frequency control circuits are provided, PLL1 606 and PLL2 608, which provide output clocks of different frequencies.

Column 5 lines 41-47. A reference clock is split into two by a programmable delay circuit 504 and fed to separate inputs of the two PLLS. Each PLL adjusts the phase and/or frequency of its output signal to match that of the reference input. Column 5, lines 47-63. Based on the foregoing, Applicant respectfully submits that the skew detection circuit of the Kurd reference does not even remotely allude to a jitter cycle delay compensation circuit that is coupled to a SYNC sampling compensation circuit, wherein the jitter cycle delay compensation circuit operates to tap a conditioned SYNC pulse signal as currently claimed. Accordingly, Applicant respectfully submits that the base claim 1 is allowable over the Price and Kurd references".

The Examiner disagrees and asserts, that, as indicated in the previous office action, that both references are consider together and Kurd clearly discloses that his application has the motivation of synchronization minimizing the skew and jitter in multiple clock domains (column 1 lines 46-48 ", *inter alia*, the phase aligner may not be sufficiently accurate (achieve low skew and jitter) at high clock frequencies "and column 2 lines 13-20, *inter alia*, "The circuit is particularly versatile because it can be used essentially unaltered in a wide range of phase alignment applications, including for instance, the dynamic adjustment of phase in different branches of a clock distribution network, reduction of static phase error in a phase locked loop (PLL) output, minimizing skew between multiple clock domains, and tuning the final clock output drivers of a clock distribution network").

As per claim 10:

The Applicant contends, "Applicant: respectfully traverses the pending 103 rejection of the base claim 10 and offers the following arguments in support. As currently constituted, the base claim 10 involves, inter alia, (i) sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion; and (ii) if the SYNC pulse signal is sampled to contain an anomalous condition during a predetermined time period, removing the anomalous condition by activating appropriate SYNC correct control logic. As discussed in detail hereinabove, the applied language of the Price reference at column 9, lines 37-42 and lines 65-67 does not teach, suggest or even remotely allude to sampling a SYNC pulse signal. Further, the Price reference does not disclose or suggest removing of any anomalous condition in the sampled SYNC pulse signal by activating appropriate SYNC correct control logic, as currently claimed.

The Examiner disagrees and asserts, that, as indicated in the previous office action that both references are consider together and the suggestion/motivation for doing so would have been to prevent the lost of synchronization avoiding the use of a sequence of predetermined zeros (Meagher figure 2, column 2 lines 30-31); a signal is sampled to contain an anomalous condition during a predetermined time period (all zeros), removing the anomalous condition by activating appropriate SYNC correct control logic (insert one in the second position).

The Applicant contends, "The Meagher reference is directed to a scheme for converting an incoming asynchronous data signal into an outgoing synchronous data

signal and vice versa in a data communication system such as the T1 carrier system that operates with a DS-1 signal. Column 1, lines S-41. In order to maintain maximum throughput on a T1 line, the one's density requirement must be compiled with- Accordingly, a channel bank's Line Interface Unit (LIU) provides one's density control by inserting a one in bit 2 whenever the other bits in the Ds word are all zeros. Column 2, lines 30-31. Applicant respectfully submits that insertion of a one to maintain a certain density requirement in a T1 data communication system does not suggest or allude to sampling a SYNC pulse signal and removing an anomalous condition therein by activating appropriate SYN correct control logic. The combined teachings of the Price and Meagher references fail to teach or suggest all the limitations of the base claim 10 as required under MPEP 52143. Additionally, even if the teachings of the applied references were to be combined, there cannot be a reasonable expectation of successfully obtaining Applicant's claimed invention because the operating conditions of a T1 transmission line (in the Meagher reference) are vastly different from those of the asynchronous subsystems within a computer as disclosed in the price reference. Accordingly, Applicant respectfully submits that the base claim 10 is allowable over the Price and Meagher references.

The Examiner disagrees and asserts, that, as indicated in the previous office action that both references are consider together and the suggestion/motivation for doing so would have been to prevent the lost of synchronization avoiding the use of a sequence of predetermined zeros (Meagher figure 2, column 2 lines 30-31); a signal is sampled to contain an anomalous condition during a predetermined time period (all

zeros), removing the anomalous condition by activating appropriate SYNC correct control logic (insert one in the second position). This technique is well know in the Synchronization field to avoid the loss of Synchronization. Meagher also indicates that , *inter alia*, "in order to insure reliable recovery of the clock on an AMI (alternate mark inversion) encoded T1 line, there is a one's density requirement in which no more than 14 consecutive zero bits are transmitted, so that the T1 receiver will stay locked onto the signal. The T1 system only guarantees 14 bits of time synchronization".

As per claim 14:

The Applicant contends, "Again, Applicant respectfully traverses the pending 103 rejection of the base claim 14 as applied above and offers the following arguments in support. As discussed previously, the applied language of the price reference at column 9, lines 37-42 and lines 65-67 does not teach, suggest or even remotely allude to sampling a SYNC pulse signal. Further, the applied language at column 7, lines 46-48 does not teach suggest or allude to determining a clock state indicative of a phase difference between first and second clock signals. Rather, a frequency synthesizer with waveform sequencer 54 (see Figure 7) is described which as in data communication with CPU 58 via a first SYNC bus 78 and in data communication with Memory Controller 62 via a Second SYNC bus 82. The function of the waveform sequencer is further described in reference to a particular embodiment of waveform sequencer 132 shown in Figure 8. As shown therein waveform sequencer 132 generates multiple frequency clocks, CLK 1 and CLK 2, as well as multiple SYNC phases. See also column 9, lines 15-30. Applicant accordingly submits that the applied language provides no suggestion

of determining a clock state indicative of a phase difference between first and second clock signals as claimed. On the other hand, application of the Kurd reference does not cure the deficiency of the Price reference when applied in combination therewith. Although it is provided in Kurd that an adjusted reference clock is obtained by delaying a reference clock signal in accordance with a first count (column 5, lines 10-16), there is no teaching or suggestion with respect to determining a clock state and re-positioning a SYNC pulse signal based on the clock state. Accordingly even if the two references were to be combined, they fail to teach or suggest all the limitations of the base claim 14".

The Examiner disagrees and asserts, that, as indicated in the previous office action, Price discloses a method and apparatus for phase aliment using a SYNC pulse, *inter alia*, "The first clock signal and the second clock signal are generated such that the two signals have a fixed predetermined timing relationship relative to one-another over a clock frame period to minimize the setup time and hold time. In addition, for each clock frame period, the clock generation circuit generates a first sync pulse to signal the first subsystem that timing alignment is established between the first clock and the second clock and a second sync pulse to signal the second subsystem that timing alignment between the first clock and the second clock has occurred." (column 2 lines 18-29). Furthermore Kurd indicates, *inter alia*, "A skew detection circuit 104 is used by each pair of branches, to align the phases of the clock signals at the output of the branches. For instance, the inputs to the circuit 104a are provided by respective programmable delay circuits 404a and 404b. The delay presented by each of these

delay circuits is variable and may be adjusted according to the count value obtained from the respective output of the circuit 104a. In this particular example, the delay presented by each delay circuit increases in response to an increase in the count value" (column 5 lines 1-9).

As per the dependent claims:

The Applicant contends, "Dependent claims 2-9 depend from the base claim 1 and introduce additional limitations therein. Dependent claims 11-13 depend from the base claim 10 and introduce additional limitations therein. Finally, dependent claims 15-19 depend from the base claim 14 and introduce additional limitations therein. Accordingly, these dependent claims are allowable over the Price, Kurd and Meagher reference, in any combination, based on the foregoing analysis regarding their respective base claims. Also, as pointed out earlier, three other references, the Kim reference, the Langendorf reference and the Magro references are applied in one or more combinations with the references used against the base claims in rejecting some of the pending dependent claims. The Kim reference is directed to a delay locked loop of a memory device (DRAM). The Langendorf reference is directed to a programmable secondary clock generator. The Magro reference is directed to synchronizing data between differing clock domains. Applicant respectfully submits that these additional references are of no avail when applied in combination with one or more of the Price Kurd and Meagher references against the base claims. Accordingly, it is believed that the dependent claims are also allowable over the entire art made of record".

The Examiner disagrees and asserts, that, as indicated in the previous office the additional references are valid when applied in combination with one or more of the Price, Kurd and Meagher references against the base claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 14-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), and further in view of Kurd (US 6622255).

As per claim 1 Price discloses a sampling compensation circuit operable to condition a SYNC pulse signal, wherein said SYNC pulse signal is based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67). Price doesn't disclose a jitter cycle delay compensation circuit coupled to said sampling compensation circuit, said jitter cycle delay compensation circuit operating to tap said SYNC pulse signal after a predetermined delay based on a skew difference between said first and second clock signals. Kurd discloses a jitter cycle delay compensation circuit coupled to said sampling compensation circuit, said jitter cycle delay compensation circuit operating to tap said SYNC pulse signal after a predetermined delay based on a skew difference between said first and second clock signals (figure 6

column 5 lines 41-44). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18). Therefore, it would have been obvious to combine Price and Kurd to obtain the invention as specified in claim 1.

As per claim 2 Price also discloses a plurality of multiplexers arranged in series, each multiplexer operating to receive an input through a timing register associated (figure 11 column 12 lines 57-63). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18). Therefore, it would have been obvious to combine Price and Kurd to obtain the invention as specified in claim 2.

As per claim 3 Price also discloses that the multiplexers are operable to insert a logic high condition in said SYNC pulse signal when said SYNC pulse signal is sampled to contain a plurality of logic lows during a predetermined time window (figure 11 column 12 line 63 to column 13 line7). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kurd with

the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18). Therefore, it would have been obvious to combine Price and Kurd to obtain the invention as specified in claim 3.

As per claim 14 Price (US 5450458) discloses sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67); determining a clock state indicative of a phase difference between said first and second clock signals (figure 7 block 74 column 7 lines 46-48); Price doesn't disclose re-positioning the SYNC pulse signal based on said clock state and if the SYNC pulse signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state. Kurt discloses re-positioning the SYNC pulse signal based on said clock state and if the SYNC pulse signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state (figure 5 column 5 lines 10-16). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the delay system circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18).

Therefore, it would have been obvious to combine Price and Kurd to obtain the invention as specified in claim 14.

As per claim 15 Kurd also discloses adding at least an extra clock cycle when said clock state indicates that said first clock signal lags with respect to said second clock signal by a predetermined amount (figure 1 column 2 lines 44-46 column2 line 63 to column 5 line 5). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the delay system circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18). Therefore, it would have been obvious to combine Price and Kurd to obtain the invention as specified in claim 15.

As per claim 16 Kurd also discloses deleting at least an extra clock cycle when said clock state indicates that said second clock signal lags with respect to said first clock signal by a predetermined amount (figure 1 column 2 lines 46-48 column2 line 63 to column 5 line 5). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the delay system circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18). Therefore, it would have been obvious to combine Price and Kurd to obtain the invention as specified in claim 16.

As per claim 19 Price also discloses that the first and second clock signals comprise a core clock and a bus clock in a computer system (figure 7 blocks 58 and 82 column 9 lines 46-51 and 56-62). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the delay system circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18). Therefore, it would have been obvious to combine Price and Kurd to obtain the invention as specified in claim 19.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), further in view of Kurd (US 6622255) and further in view of Meagher (US 5054020). Price and Kurd disclose claim 2. Price and Kurd don't teach that the multiplexers operable to insert a [010] sequence in the SYNC pulse signal when the SYNC pulse signal is sampled to be all zeros during a predetermined time window. It is very well known and Meagher discloses to insert a [010] sequence the signal is sampled to be all zeros during a predetermined time window (figure 2, column 2 lines 30-31). Price, Kurd and Meagher teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate synchronization technique disclosed by Meagher with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to prevent the lost of synchronization avoiding the use of a sequence of predetermined

zeros (Meagher figure 2, column 2 lines 30-31). Therefore, it would have been obvious to combine Price and Kurd to obtain the invention as specified in claim 4.

Claims 5-9 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), further in view of Kurd (US 6622255), and further in view of Kim (US 6396322).

As per claim 5 Price and Kurd disclose claim 1. Price and Kurd don't teach that the jitter cycle delay compensation circuit with a series of delay registers, each operating to delay said SYNC pulse signal by a predetermined amount of time; and a multiplexer operable to select a delayed SYNC pulse output generated from said series of delay registers. Kim discloses a jitter cycle delay compensation circuit with a series of delay registers, each operating to delay said SYNC pulse signal by a predetermined amount of time, and a multiplexer operable to select a delayed SYNC pulse output generated from said series of delay registers (figure 6 page 3 paragraph [0032]). Price, Kurd and Kim teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kim with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to reduce the complexity of the jitter delay compensation unit, using only de pre-determinate number of delay elements that will eliminate the skew in a pre-determined number of cycles (Kim figure 6 page 3 paragraph [0031]). Therefore, it would have been obvious to combine Price, Kurd and Kim to obtain the invention as specified in claim 5.

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As per claim 6 Price, Kurd and Kim disclose claim 5. Kim also discloses that the series of delay registers comprises eight registers (Kim figure 6 page 3 paragraph [0032]). Price, Kurd and Kim teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kim with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to reduce the complexity of the jitter delay compensation unit, using only de pre-determinate number of delay elements that will eliminate the skew in a pre-determined number of cycles (Kim figure 6 page 3 paragraph [0031]). Therefore, it would have been obvious to combine Price, Kurd and Kim to obtain the invention as specified in claim 6.

As per claim 7 Price, Kurd and Kim disclose claim 5. Kurd also discloses a control signal generated by a state/correct block responsive to a skew difference between said first and second clock signals (Kurd figure 2 column 4 lines 25-29). Price, Kurd and Kim teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kim with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to reduce the complexity of the jitter delay compensation unit, using only de pre-determinate number of delay elements that will eliminate the skew in a pre-determined number of cycles (Kim figure 6 page 3 paragraph [0031]). Therefore, it would have been obvious to combine Price, Kurd and Kim to obtain the invention as specified in claim 7.

As per claim 8 Price, Kurd and Kim disclose claim 7 Kurd also discloses a state/correct block is coupled to a phase detector operating to detect said skew difference between said first and second clock signals (Kurd figure 1 block 108 column 2 lines 42-44). Price, Kurd and Kim teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kim with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to reduce the complexity of the jitter delay compensation unit, using only de pre-determinate number of delay elements that will eliminate the skew in a pre-determined number of cycles (Kim figure 6 page 3 paragraph [0031]). Therefore, it would have been obvious to combine Price, Kurd and Kim to obtain the invention as specified in claim 8.

As per claim 9 Price, Kurd and Kim disclose claim 7 Kim also discloses that control signal is stored in a flip-flop (Kim figure 6 page 3 paragraph [0032]). Price, Kurd and Kim teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kim with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to reduce the complexity of the jitter delay compensation unit, using only de pre-determinate number of delay elements that will eliminate the skew in a pre-determined number of cycles (Kim figure 6 page 3 paragraph [0031]). Therefore, it would have been obvious to combine Price, Kurd and Kim to obtain the invention as specified in claim 9.

As per claim 17 Price and Kurd teach claim 14. Price and Kurd didn't teach delaying by propagating said SYNC pulse signal through a series of delay registers operable to be selected by a multiplexer in response to a control signal corresponding to the clock state. Kim discloses a jitter cycle delay compensation circuit with a series of delay registers, each operating to delay said SYNC pulse signal by a predetermined amount of time, and a multiplexer operable to select a delayed SYNC pulse output generated from said series of delay registers (figure 6 page 3 paragraph [0032]). Price, Kurd and Kim teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kim with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to reduce the complexity of the jitter delay compensation unit, using only de pre-determinate number of delay elements that will eliminate the skew in a pre-determined number of cycles (Kim figure 6 page 3 paragraph [0031]). Therefore, it would have been obvious to combine Price, Kurd and Kim to obtain the invention as specified in claim 17.

As per claim 18 Price, Kurd and Kim teach claim 17. Kim also discloses that control signal is stored in a flip-flop (Kim figure 6 page 3 paragraph [0032]). Price, Kurd and Kim teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kim with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to reduce the complexity of the jitter delay compensation unit, using only de pre-determinate number

of delay elements that will eliminate the skew in a pre-determined number of cycles (Kim figure 6 page 3 paragraph [0031]). Therefore, it would have been obvious to combine Price, Kurd and Kim to obtain the invention as specified in claim 18.

Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), and further in view of Meagher (US 5054020).

As per claim 10 Price discloses a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67). Price doesn't disclose that when the signal contains an anomalous condition during a predetermined time period, removing said anomalous condition by activating appropriate SYNCH correct control logic. It is very well known and Meagher discloses that when the signal contains an anomalous condition during a predetermined time period, removing said anomalous condition by activating appropriate SYNCH correct control logic (figure 2, column 2 lines 24-55). Price and Meagher teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate synchronization technique disclosed by Meagher with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to prevent the lost of synchronization avoiding the use of a sequence of predetermined zeros (Meagher figure 2, column 2 lines 24-55). Therefore, it would have been obvious to combine Price and Meagher to obtain the invention as specified in claim 10.

As per claim 12 Price also discloses that the SYNC pulse signal is generated when a rising edge in said first clock signal coincides with a rising edge in said second clock signal (figures 13 and 14 point 1 column 14 line 62 to column 15 line 8). Price and Meagher teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate synchronization technique disclosed by Meagher with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to prevent the lost of synchronization avoiding the use of a sequence of predetermined zeros (Meagher figure 2, column 2 lines 24-55). Therefore, it would have been obvious to combine Price and Meagher to obtain the invention as specified in claim 12.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), further in view of Meagher (US 5054020) and further in view of Langendorf (US 5256994). Price and Meagher disclose claim 10. Price and Meagher don't specifically disclose that the second clock signal is generated by a phase-locked loop (PLL) based on said first clock signal. It is very well known and Langendorf disclose the case where the second clock signal is generated by a phase-locked loop (PLL) based on said first clock signal (figure 2 column 5 lines 53-55). Price, Meagher and Langendorf teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the use of a PLL to generate the second clock signal as disclosed by and Langendorf with the SYNC pulse signal disclosed by Price and Meagher. The suggestion/motivation for doing so would have to provide synchronization between the two clock domains (Langendorf

abstract). Therefore, it would have been obvious to combine Price, Meagher and Langendorf to obtain the invention as specified in claim 11.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), further in view of Meagher (US 5054020) and further in view of Magro (US 6516362). Price and Meagher disclose claim 10. Price and Meagher don't specifically disclose that the SYNC pulse signal is generated when a rising edge in said first clock signal coincides with a rising edge in said second clock signal. Magro specifically discloses that SYNC pulse signal is generated when a rising edge in said first clock signal coincides with a rising edge in said second clock signal (figure 3-6 column 8 lines 25-33). Price, Meagher and Magro teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the generation of the SYNC signal when a rising edge in said first clock signal coincides with a rising edge in said second clock signal as disclosed by and Magro with the SYNC pulse signal disclosed by Price and Meagher. The suggestion/motivation for doing so would have to provide communication among multiple computer devices operating at different frequencies utilizing clock synchronization (Magro abstract). Therefore, it would have been obvious to combine Price, Meagher and Magro to obtain the invention as specified in claim 12.

Allowable Subject Matter

Claim 20 allowed.

Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: claims 13 and 20 are allowed because the references cited fail to teach, as applicant has, that when said SYNC pulse signal is sampled to indicate a duplicate logic high condition during a predetermined time period, masking the duplicate logic high condition, as the applicant has claimed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
4-25-2005

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MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER